REMARKS

At pages 3-5 of the Office Action, the Examiner rejects claims 1, 3, 5, 7-9 and 13-14 under 35 USC 102(e) as being anticipated by Ker et al. (US Patent No. 6,514,839). Moreover, at page 5, claim 2 is rejected under 35 USC 103(a) as being unpatentable over Ker et al. '839 in view of Ker et al. (US 2002/0076876). At page 6, claim 4 is rejected under 35 USC 103(a) as being unpatentable over Ker et al. '839 in view of Chuang et al. (US Patent No. 6,008,080). At page 7, claim 6 is rejected under 35 USC 103(a) as being unpatentable over Ker et al. '839 in view of Kuo (US Patent No. 6,268,256). Claims 10-12 are rejected under 35 USC 103(a) as being unpatentable over Ker et al. '839 in view of Hsu (US Patent No. 6,100,141). These rejections are respectfully traversed.

Ker et al. '839, Ker et al. '876, Chuang et al., Kuo and Hsu, standing alone or in combination, fail to disclose, teach, or suggest, *inter alia*, the following features recited by claim 1 of the present application:

"at least one first island, formed within and completely surrounded by the first drain/source region...".

Ker et al. '839 discloses an implanting method for forming high voltage tolerant ESD protection devices for deep-submicron CMOS process activated between LDD implanting and forming sidewall spacers. Ker et al. '839 does not disclose a "first island, formed within and completely surrounded by the first drain/source region", as recited by claim 1 of the present application.

At pages 3-4 of the Office Action, the Examiner simply copies limitations of claim 1 and asserts that they are disclosed by Figs. 6H and 20 and cols. 9-12, lines 59-67, 1-67, 1-8 and 30-63 of Ker et al. The Examiner does not specify what elements in Ker et al. correspond to each limitation of claim 1. It is unclear how the cited passages in Ker et al. teach all limitations of claim 1.

At page 4, paragraph 1, the Examiner identifies the gate electrodes 64 in Ker et al. as the first island in the claimed invention. The Applicants disagree. At col. 10, lines 3-8, Ker et al. teaches "[t]he next step 51 is to form a gate-oxide layer GOX and a gate electrode layer of doped conductive poly, that is patterned into gate electrodes 64 by a patterned photoresist mask PR1, as that shown in FIG. 6B. Then mask PR1 is stripped away form the device 60."

In Ker et al. '839, Figs. 8, 12, 15 and 18 are layout top view of MOS devices. In Figs. 8, 12, 15 and 18, the gate electrodes traverse across the active region. That implies the gate electrodes 64 in figures 6H and 20 also traverse across the active region. Therefore, **the gate electrodes 64 are not the at least one first island** in the claimed invention.

Since Ker et al. teach that the gate electrodes traverse across the active region, the active region is divided into separated drain/source regions by the gate electrodes. The gate electrodes are not the at least one first island **formed on the first drain/source region.** To more clearly recite this feature, the Applicants have amended claim 1 to read "at least one first island, formed within and completely surrounded by the first

drain/source region".

Ker et al. '876, Chuang et al., Kuo and Hsu are cited only with respect to features of the dependent claims. The Examiner does not show that the above-quoted features of claim 1 are taught or suggested by these references. Moreover, Chuang, Kuo and Hsu are related to logic device characteristic improvement, not for the purpose of ESD protection. Thus, the Applicants believe that it would not have been obvious to combine these references with Ker et al. '839, without first reading the disclosure of the present application.

MPEP 2131 states that a "ciaim is anticipated only if **each and every element** as set forth in the claim is found, either expressly or inherently described, in a single prior art reference," quoting *Verdegaal Bros v. Union Oil Co. of California*, 814 F.2d 628, 631 (Fed. Cir. 1987). Under MPEP 2143, to establish a prima facie case of obviousness, the prior art reference (or references when combined) must teach or suggest all the claim limitations. Since the cited references do not teach or suggest the above-quoted features of claim 1, the Applicants believe that claim 1 is patentable. Claims 2-14 are also patentable, at least by virtue of their dependency from claim 1. Moreover, these claims are patentable by virtue of the additional limitations recited therein.

For example, claim 2 recites, in part, "two breakdown-enhanced layers with the same depth and the same dosage on different sides of the channel region". It is clear that the cited references nowhere teach this feature.

The Applicants have attempted to address all of the issues raised by the Examiner in the Office Action as the Applicants understand them. The Applicants believe that the Application is now in condition for allowance. If any point requires further explanation, the Examiner is invited to telephone Troy Cai at (323) 934-2300 or e-mail Troy Cai at tcai@ladasparry.com.

The Commissioner is authorized to charge any additional fees which may be required or credit overpayment to deposit account No. 12-0415. In particular, if this response is not timely filed, then the Commissioner is authorized to treat this response as including a petition to extend the time period pursuant to 37 CFR 1.136 (a) requesting an extension of time of the number of months necessary to make this response timely filed and the petition fee due in connection therewith may be charged to deposit account no. 12-0415.

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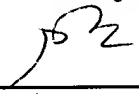
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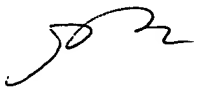

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